**Logic - Laboratory**

1. **Instructions**

Work in groups of four. You have two supervised laboratory sessions to work on the practical - Outstanding sections of the laboratory must be completed in your own time.

The completed laboratory should be uploaded into the course's upload system. Incomplete work will not be marked. You should print out the [Marking Scheme](http://staffweb.cms.gre.ac.uk/~sp02/logic/MarkingScheme.html) and bring a print out of your group's completed laboratory report to the next laboratory session.

1. **Objectives**
   * To determine the logic function of six fundamental gates.
   * To become familiar with the analysis and design of simple combinational logic circuits.
   * To determine the operation and functionality of basic sequential logic circuits.
   * To be able to relate the circuits to the internal architecture of Central Processing Units
2. [**Apparatus**](http://staffweb.cms.gre.ac.uk/~sp02/equipment/equipmentlist.htm)
   * Analogue Oscilloscope + Two oscilloscope probes, BNC to BNC Cable, BNC "T" adaptor, BNC to probe clips cable
   * Breadboard
   * Crocodile Clips Software
   * Function Generator
   * IDC10 Cable x 2
   * Jump Wire Kit
   * Laboratory DC Power Supply + Two sets of Banana leads
   * Multi meter and Banana plug test probes
   * Switch Light Box, Logic Box
   * Dual Seven Segment Display
3. **Introduction**

Digital logic may be divided into two classes: combinational logic, in which the logical outputs are determined by the logical function being performed and the logical input states at that particular moment; and sequential logic, in which the outputs also depend on the prior states of those outputs. Both classes of logic are used extensively in all digital computers.

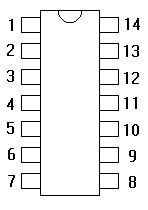
1. **Procedure**
   * **Logic Gates**

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| Logic Box | The objective of this exercise is to determine the logic function of six fundamental gates.   Identify the box with the six integrated circuits labelled A to F.  Set the variable output of the laboratory DC power supply to 9 volts and connect to the box.  The two switches set the logic states of signals to be applied to each Integrated circuit (IC), while the LEDs (Light Emitting Diodes) are used to indicate the logic states of the individual integrated circuits outputs.  Change the two switches through all possible combinations, and make a note of the LED outputs  A LED in the ON state corresponds to logic 1. |

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| TASK 0  Determine the logic function of the six integrated circuits labelled A B C D E & F. For each integrated circuit, determine the truth table, the Boolean equation and the circuit diagram.   |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | | S1 | S2 | A | B | C | D | E | F | |  |  |  |  |  |  |  |  | |  |  |  |  |  |  |  |  | |  |  |  |  |  |  |  |  | |  |  |  |  |  |  |  |  | |

* + **Combinational Logic**

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| Combinational Logic Set Up | Identify the breadboard with twelve integrated circuits and two IDC 10 pin ribbon cable to breadboard adapters.  Construct the circuit on the left. The IDC10 cables connect from the breadboard to to the switches' and  LED's IDC connections of the switch light box. |

* + **Integrated Circuit Identification**
  + The integrated circuits have a number stamped on the top, enabling their function to be identified. Input and output signals are associated with a pin number. Pin numbers range from 1 up to 14 for the integrated circuits you will be using. A small notch at the end of each integrated circuit orientates the pin numbering. If you are have difficulty, the integrated circuits should be located on the breadboard as shown in the [breadboard image](http://staffweb.cms.gre.ac.uk/~sp02/logic/breadboard2big.htm).
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  + In addition to the various inputs and outputs, the integrated circuits require 5 volts at the Vcc (Voltage Collector Collector) pin 14 and 0 volts at the Gnd (Ground) pin 7.
  + **Integrated Circuits Diagrams**

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| http://staffweb.cms.gre.ac.uk/~sp02/logic/images/NANDchip.gif | http://staffweb.cms.gre.ac.uk/~sp02/logic/images/NORchip.gif | http://staffweb.cms.gre.ac.uk/~sp02/logic/images/NOTchip.gif |
| NAND gate (Type number SN74LS00) | NOR gate (Type number SN74LS02) | NOT gate (Type number SN74LS04) |
| http://staffweb.cms.gre.ac.uk/~sp02/logic/images/ANDchip.gif | http://staffweb.cms.gre.ac.uk/~sp02/logic/images/ORchip.gif | http://staffweb.cms.gre.ac.uk/~sp02/logic/images/XORchip.gif |
| AND gate (Type Number SN74LS08) | OR gate (Type Number SN74LS32) | XOR gate (Type Number SN74LS86) |
| http://staffweb.cms.gre.ac.uk/~sp02/logic/images/AND3chip.gif | http://staffweb.cms.gre.ac.uk/~sp02/logic/images/DFlipFlopChip.gif | http://staffweb.cms.gre.ac.uk/~sp02/logic/images/JKFkipFlopChip.gif |
| AND gate (Type Number SN74LS11) | D Type Flip Flop (Type Number SN74LS74A) | JK Flip Flop (Type Number SN74LS107A) |

* + **Switch Light Box Connections**
  + Connections to and from the inputs and outputs of circuits constructed on the breadboard to the switches and LEDs of the switch  light box are made via the two IDC 10 pin ribbon cables to breadboard adapters on the breadboard.
  + In the example depicted, the IDC connector is connected via the IDC10 cable to the LEDs connection on the switch light box. A logic one (5 V) on the blue and red wires and logic zero (0 V) on the green wire would turn LED 0 and LED 3 on and turn LED 4 off switch light box on .
  + The Vcc connection is not used in the switch light box and therefore no connection should be made to this pin. However the Gnd pin should be connected to the Gnd rail on the breadboard as shown.

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| IDC Interface | IDC Example |
| Pin Numbering of the IDC Breadboard Adapter (seen from above) | IDC Breadboard Adapter Connection Example |  |

* + **Mystery Circuit**
  + Construct the circuit below. Connect the circuit's inputs to switches 7, 6 and 5 and the outputs to LED's 7 and 6 of the switch light box. Determine the truth table of the circuit. What function does this circuit perform?

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| Mystery Circuit | |  |  |  |  |  | | --- | --- | --- | --- | --- | | S7 | S6 | S5 | L7 | L6 | | 0 | 0 | 0 |  |  | | 0 | 0 | 1 |  |  | | 0 | 1 | 0 |  |  | | 0 | 1 | 1 |  |  | | 1 | 0 | 0 |  |  | | 1 | 0 | 1 |  |  | | 1 | 1 | 0 |  |  | | 1 | 1 | 1 |  |  | |

* + Confirm the operation of the circuit by calculating the circuit's operation with a truth table and constructing the circuit in Crocodile Clips.
  + In Crocodile Clips increase the functionality of the circuit by joining three of the circuits together. Give examples of the combined circuits operation.

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| TASK 1   Demonstrate the circuit's operation to the tutor, and upload to your logbook, the truth table, a description of the function of the circuit, clearly indicating the purpose the inputs and outputs.   A circuit diagram of the three of the circuits connected together with the function of all inputs and outputs clearly marked - state where any unused input or outputs would be connected to within a computer. Give three examples showing the circuit's operation. |

* + **The Social Committee**
  + Three potential members of a Social Committee, John, Mary and Susan are subject to the following rules: -
    - John will only serve if Mary also serves.
    - Mary Will only serve if Susan doesn't serve.
    - At least one of the women must serve.

Use a Karnaugh map to design and implement a logic circuit that indicates the allowed combination of committee members.

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| TASK 2   Demonstrate the circuit's operation to the tutor and upload to your logbook, the truth table, the Karnaugh map and the circuit diagram. |

**Seven Segment Display**

A Binary Coded Decimal (BCD) seven segment decode circuit has 4 inputs and has seven output. The inputs represent a number between 0 and 9, and each of the seven outputs corresponds to one of seven LED's in a seven-segment display. The laboratory's IDC dual seven segment display is shown below .

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| Seven Segment | IDC Pins |
| A logic 1 illuminates the segment. Bit seven is used as a multiplex bit to select each of the seven segment displays - setting bit 7 to 0 displays the most significant character on the display **a**nd setting bit 7 to 1 least significant character on the display. | |

A BCD 7 segment decode circuit's truth table is shown below.

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| Digit | Inputs | | | | Outputs | | | | | | | Output    Seven Segment |
| S3 | S2 | S1 | S0 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | LED 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | LED 1 |
| 2 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | LED 2 |
| 3 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | LED 3 |
| 4 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | LED 4 |
| 5 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | LED 5 |
| 6 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | LED 6 |
| 7 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | LED 7 |
| 8 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | LED 8 |
| 9 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | LED 9 |
| - | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | LED Off |
| - | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | LED Off |
| - | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | LED Off |
| - | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | LED Off |
| - | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | LED Off |
| - | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | LED Off |

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| TASK 3   Construct the Karnaugh map for the segment controlled by 'bit 5' and implement the circuit.  Connect the switch light box and the dual seven segment display to the breadboard and demonstrate the circuit's operation to the tutor. Upload the Karnaugh map and circuit diagram to your logbook |

* + **Sequential Logic**

Combinational circuits provide no memory or state information, which requires a more complex from of digital logic - the sequential circuit.  Sequential logic differs from combinational logic in that the output of the logic device is dependent not only on the present inputs to the device, but also on past inputs; i.e. the output depends on the present internal state and the present inputs. This implies that a sequential logic device has memory of  its previous inputs.

**SR Latch**

Construct the circuit below. Draw all of the timing diagrams that depict the relationship of  S, R and Q. Determine the truth table of the circuit.

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| http://staffweb.cms.gre.ac.uk/~sp02/logic/images/FlipFl2.gif | |  |  |  | | --- | --- | --- | | S | R | Qn+1 | | 0 | 0 |  | | 0 | 1 |  | | 1 | 0 |  | | 1 | 1 |  | |

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| TASK 4   Upload to your logbook, the truth table and timing diagrams. State the purpose of the circuit. |

**Clocked SR Latch**

In n Crocodile Clips construct the circuit below. Draw the timing diagram showing the Clock, S, R and Q and determine the truth table of the circuit.

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| http://staffweb.cms.gre.ac.uk/~sp02/logic/images/logic13.gif | |  |  |  |  | | --- | --- | --- | --- | | Clk | S | R | Qn+1 | | 0 | 0 | 0 |  | | 0 | 0 | 1 |  | | 0 | 1 | 0 |  | | 0 | 1 | 1 |  | | 1 | 0 | 0 |  | | 1 | 0 | 1 |  | | 1 | 1 | 0 |  | | 1 | 1 | 1 |  | |

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| TASK 5   Upload to your logbook, the truth table, timing diagram and discuss the function of the clock, identifying any advantages/disadvantages with respect to the SR latch. |

**Clocked D Latch**

Construct the circuit below. Draw the timing diagram showing the Clock, D and Q and determine the truth table of the circuit.

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| http://staffweb.cms.gre.ac.uk/~sp02/logic/images/logic14.gif | |  |  |  | | --- | --- | --- | | Clk | D | Qn+1 | | 0 | 0 |  | | 0 | 1 |  | | 1 | 0 |  | | 1 | 1 |  | |

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| TASK 6   Upload to your logbook, the truth table, timing diagram and discuss any advantages/disadvantages of this circuit with respect to the clocked SR latch. |

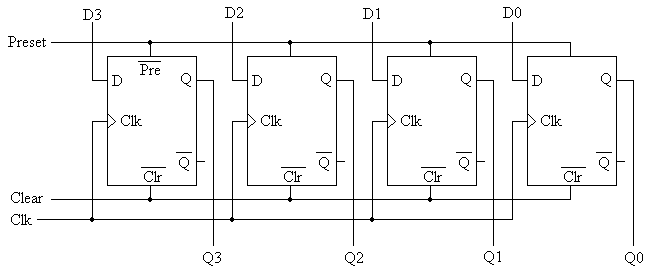
**D Flip Flop**

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| D Type | |  |  |  | | --- | --- | --- | | Clk | D | Qn+1 | |  | 0 |  | |  | 1 |  | |  | 0 |  | |  | 1 |  | | Use a D type flip flop from the SN74LS74A package (Turn preset and clear off - Note the bar!). In Crocodile Clips, the circuit does not have Preset or Clear.   Draw the timing diagram showing the Clock, D and Q and determine the truth table of the circuit (You will need to think carefully how to annotate the Clk in the truth table) |

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| TASK 7  Upload to your logbook, the truth table and timing diagram. Apart form the preset and clear option on this device, state how this device's behaviour differs from the clocked D Latch above. With the aid of timing diagrams, discuss any advantages/disadvantage between the two. |

**Registers**

Construct the circuit below and establish it functionality.



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| TASK 8   Discuss where this circuit could be employed within a computer. |

**JK Flip Flop**

Construct the circuit below. Draw the timing diagram showing the Clock, J, K and Q and determine the truth table of the circuit.

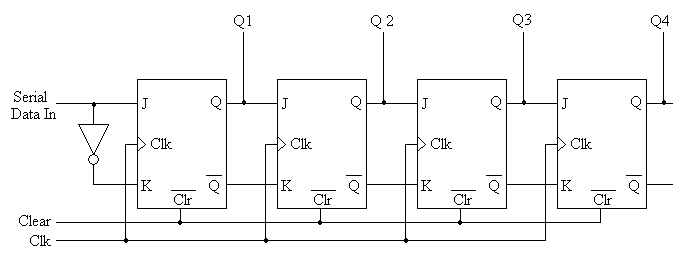
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| http://staffweb.cms.gre.ac.uk/~sp02/logic/images/logic18.gif | |  |  |  | | --- | --- | --- | | J | K | Qn+1 | | 0 | 0 |  | | 0 | 1 |  | | 1 | 0 |  | | 1 | 1 |  | |

After establishing the circuit's operation set J and K to 1, disconnect the switch on the clock input and connect the TTL output of the function generator via a BNC (Bayonet Neill Concelman) to Probe Clips Cable to provide a clock signal to the circuit. Display on the oscilloscope the clock and Q signals. Record the oscilloscope display.

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| TASK 9  Upload the truth table, timing diagram. With relation to the master slave arrangement of the circuit discuss the circuit's operation. Discuss where this circuit could be employed within a computer. |

**Shift Register**

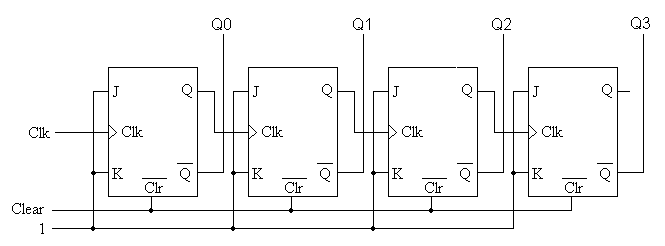
Construct the circuit below.



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| TASK 10  What functions could this circuit perform? Discuss how this circuit could perform division by 2. |

**Binary Counter**

Construct the circuit below. After testing the circuit with a switch as an input to the clock, disconnect the switch and connect the TTL output of the function generator via a BNC to probe clip cable to provide a clock signal to the circuit. Use an oscilloscope and oscilloscope probes to establish the relative relationship of the waveforms at Clk, Q0, Q1, Q2 and Q3. Draw Q0, Q1, Q2, Q3 and the Clock waveforms on the same time scale.



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| TASK 11   Upload the timing diagram showing the relative relationship of the waveforms at Clk, Q0, Q1, Q2 and Q3 Discuss where this circuit could be employed within a computer |

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| TASK 12  Identify the sections of the laboratory you have understood and demonstrate your understanding - beyond the simple level of completing the laboratory - through cognitive processes such as analysing, explaining, interpreting, and evaluating. Illustrate, by the use of examples how the laboratory contributed towards your understanding and your Degree programme.  For the sections of the laboratory in which you struggled with, or were uncertain of, identify why this was the case. Evaluate the effectiveness of your learning strategy, including factors such as, motivation, preparation, commitment, time management, communication, constraints and support. With reflection to past experience, identify how you could improve your learning and performance to overcome the barriers encountered in this laboratory such that they do not infringe upon the next laboratory you undertake.  With relation to the sections of the laboratory you encountered difficulty with, state how, and by when you intend to gain competence in these areas.  Critically appraise the laboratory; identify sections you thought were positive, facilitated your understanding and contributed to your Degree programme; identify sections that require improvement and state how and why would you change the laboratory to improve the laboratory for the next year's students. |

• [Apparatus](http://staffweb.cms.gre.ac.uk/~sp02/equipment/equipmentlist.htm) • [Technician's Guide](http://staffweb.cms.gre.ac.uk/~sp02/logic/technicianguide.html) • [Oscilloscope Guide](http://staffweb.cms.gre.ac.uk/~sp02/equipment/oscilloscopeguide.htm) • [Breadboard Guide](http://staffweb.cms.gre.ac.uk/~sp02/equipment/breadboard.htm)